Application No.: 09/974,608

Docket No.: SCEIWI 3.0-090

Alad

drawing end signal is to be received, are set for each application. A main SYNC sends the drawing enable signal to corresponding GSMs in the order of setting for an application in response to the reception of a processing request from the application, while it receives the drawing end signal from the corresponding GSMs so that the processing results of the GSMs will be displayed on the display unit.

## IN THE SPECIFICATION

CLEAN COPY OF AMENDED SPECIFICATION PARAGRAPHS:

•

[8000] According to another aspect of the present invention, there is provided a data processing system comprising: M first arbitrator means (where M is a natural number greater than one) each for arbitrating operations of corresponding N processing units (where N is a natural number greater than one), the N processing units cooperating to perform cooperative processing, second arbitrator means for arbitrating operations of the M first arbitrator means, and control means for controlling operations of the first and second arbitrator means, such that each processing unit initiates processing assigned thereto, in response to reception of an execution enable signal sent from the control means, and after execution of the processing, each processing unit sends a processing result and an execution end signal to the control means, wherein the control means has a processing table for each application, the processing table storing, in a predetermined order, identification information on one or more processing units to which the execution enable signal is to be sent, and identification information on one or more processing units from which the processing result and the execution end signal are to be received, whereby, in response to receipt of a processing request from an application, execution enable signal is sent to the one or more processing

Application No.: 09/974,608 D

Docket No.: SCEIWI 3.0-090

\$3 Cadd units and the processing result and the execution end signal are received from the one or more processing units, in the order determined by the corresponding processing table for the application.

A3

[0030] A description will now be made of an embodiment in which a data processing system according to the present invention is applied to an integrated image processing apparatus provided with two or more image processing units that carry out cooperative processing.

AH

The sub-CP 5 controls the operation of the entire GSB. The sub-CP 5 is equipped with a demultiplexer (not shown) for dividing the input data into four parts and distributing to each of the four GSMs 1 a quarter of the image data string related to a moving image to be generated. The distribution may take various forms depending on the application software run on the apparatus. For example, the whole area of an image to be finally displayed may be divided into four parts, or into four image data strings, each of which is to display a corresponding layer to be superimposed one upon another for the final image. Alternatively, image data that has combined four frames into one may be divided into four parts.

A5

[0039] The sub-NET 6 is a circuit for passing part or all of the image data string between its own GSB and another GSB. The image data string is passed mainly to balance the load of image processing among the GSBs.

A6 Cost [0040] It should be noted that merging performed by the sub-MG 3 is carried out in synchronization with an absolute time base that controls the operation of all the GSBs. In other words, the sub-MG 3 merges two or more pieces of frame image

Ab

Application No.: 09/974,608

Docket No.: SCEIWI 3.0-090

data input in synchronization with the absolute time base to generate one frame of image data.

A7

[0054] The GIF 30 arbitrates the transfer of the display lists created in the first VPU 20 and the second VPU 21 during the transfer operation. In the embodiment, the GIF 30 has an additional function for putting these display lists in the order of priority and transferring them to the GS 31 sequentially in order of precedence. Information indicative of priority of each display list is generally described in a tag field of the display list when the VPU 20 or 21 creates the display list, but the priority may be judged independently by the GIF 30.

A8

[0062] Next, a description will be made about an exemplary form of data processing executed in the integrated image processing apparatus.

A9

[0064] In the embodiment, a display sequence table TB is prepared for each application. The display sequence table TB stores in a predetermined order IDs of the GSMs 1 to which the drawing enable signal (DrawNext) is to be sent and IDs of the GSMs 1 from which the drawing end signal (DrawDone) is to be received. The display sequence table TB is provided in any one of the external storage 410 on the main CP 400 side, the data register of the main MG 200, and the data register of the main SYNC 300. In other words, the display sequence table TB is provided in a region in which the main SYNC 300 can point to the contents thereof.

Alo Cm.t [0068] The SYNC 300 points (e.g., provides) each GSM group with two indexes "Display Start" and "Display End." The index "Display Start" indicates that the GSM group is scheduled to make an image display on the display unit DP on the basis of the processing results after ending the drawing process (after

Application No.: 09/974,608 Docket No.: SCEIWI 3.0-090

Alo cincled.

receiving the drawing end signal (DrawDone)). The index "Display End" indicates that the GSM group is in such a state that it can issue the drawing enable signal for the next frame after a period of display of a one-frame image on the display unit DP. When the single buffer system is adopted, the display of the next frame image is started after completion of the display of the previous frame image. When the double buffer system is adopted, the display start processing and the display end processing are carried out at the same time. Therefore, as shown at (a) and (b) in Fig. 4, the display timing in the single buffer system is delayed by one-SYNC compared to that in the double buffer system.

AII

[0069] Next, a description will be made about an operation form of the integrated image processing apparatus configured as above. The integrated image processing apparatus operates on the presumption that an application has been loaded into the external storage 410 so that an image data string can be supplied to each GSM 1 through the main CP 400 and the sub-CP 5 in each GSB 100.

A12

[0070] The main CP 400 launches the application, and when a processing request is made from the application, it gives drawing instructions to the main SYNC 300 through the main MG 200. Upon receipt of the drawing instructions from the main CP 400, the main SYNC 300 sends the drawing enable signal (DrawNext) to corresponding GSMs 1 in the order of storage on the display sequence table TB for the application concerned.

A13

[0072] In the single buffer system, the GSM 1 executes processing steps shown at (a) in Fig. 5.

914 Cm. T [0104] Although the invention herein has been described with reference to particular embodiments, it is to be understood that